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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,440	09/30/2003	Robert M. Geffken	BUR920030025US1	2439

29505 7590 10/21/2005

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,440	GEFFKEN ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0903 & 1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 08/01/2005.

Claims 1-16 are active in this application.

Claim(s) 17-20 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 09/30/2003 and 10/27/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Remarks

3. Applicant's Declaration and arguments filed on 08/01/2005 have been fully considered, but are moot in view of the new ground(s) of rejection(s).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim(s) 1 is rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,117,276 to Thomas et al.

Regarding claim 1, Thomas discloses a semiconductor device, as shown in fig. 2A, comprising:

a first interconnect 38 adjacent a second interconnect 38 on an interconnect level (second level of interconnects);

spacers 52 formed along adjacent sides of the first and second interconnects 38; and

an air gap 53 formed between the first and second interconnects 38, the air gap 53 extending above an upper surface of at least one of the first and second interconnects 38 and below a lower surface of at least one of the first and second interconnects 38, distance between the spacers 52 defining the width of the air gap 53.

6. Claim(s) 1-3 and 7-16 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,413,852 to Grill et al.

Regarding claim 1, Grill discloses a semiconductor device, as shown in figs. 1-5, comprising:

a first interconnect 185 adjacent a second interconnect 185 on an interconnect level (see further col. 10, lines 3-29);

spacers 210 formed along adjacent sides of the first and second interconnects 185; and

an air gap 270/270' formed between the first and second interconnects 185, the air gap 270/270' extending above an upper surface of at least one of the first and second interconnects 185 and below a lower surface of at least one of the first and second interconnects 185 (see figs. 4C/D, 5D), distance between the spacers 210 defining the width of the air gap 270/270'. See also col. 4, line 50 to col. 10, line 30.

Regarding claim 2, Grill discloses the semiconductor device wherein the air gap 270/270' is self-aligned to the adjacent sides of the first and second interconnects 185. See figs. 4C/C, 5D.

Regarding claim 3, Grill discloses the semiconductor device wherein the spacers 210 adjacent the sides of the first and second interconnects 185 comprise silicon dioxide or silicon nitride. See col. 4, line 63 to col. 5, line 24; col. 6, lines 22-44.

Regarding claim 7, Grill disclose the semiconductor device further including hardmask spacers 510 self-aligned to either side of an upper portion of the air gap, wherein the air gap extends between and below the hardmask spacers 510. See figs. 5C-D, and col. 9, lines 58 to col. 10, line 29.

Regarding claim 8, Grill discloses the semiconductor device wherein the hardmask spacers comprise silicon dioxide or silicon nitride. col. 9, lines 58 to col. 10, line 29.

Regarding claim 9, Grill discloses the semiconductor device further including at least one insulative layer 250 above the interconnect level 185 and the air gap 270, and wherein the air gap 270 extends into the insulative layer 250. See figs. 1N, 2B, and col. 7, line 10 to col. 8, line 32.

Regarding claim 10, Grill discloses the semiconductor device wherein the at least one insulative layer 250 above the interconnect level and the air gap comprises silicon nitride or silicon carbon nitride as a capping layer for the interconnect and silicon dioxide or fluorinated silicon dioxide as an insulative layer above the capping layer. See col. 7, line 10 to col. 8, line 32.

Regarding claim 11, Grill discloses the semiconductor device further including hardmask spacers 250 self-aligned to either side of an upper portion of the air gap 270/270', and an insulative layer 280 above the interconnect level, the air gap and the hardmask spacers, and wherein the air gap extends between the hardmask spacers and upward into the insulative layer 280. See figs. 2A-B.

Regarding claim 12, Grill discloses the semiconductor device wherein the first and second interconnects are formed by a damascene or dual damascene process. See col. 2, lines 1-9; col. 5, lines 33-53.

Regarding claim 13, Grill discloses the semiconductor device wherein the first and second interconnects comprise copper, aluminum, tungsten or gold. See col. 5, lines 41-43.

Regarding claim 14, Grill discloses the semiconductor device further including, beneath one of the first and second interconnects, an etch stop layer 110/130 positioned over at least one underlying via insulator level, and below the underlying via insulator, a second interconnect level. See figs. 1-5. See also col. 10, lines 10-29.

Regarding claim 15, Grill discloses the semiconductor device further including, between the at least one underlying via insulator level and the second interconnect level, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer. See col. 4, lines 50-58. See also col. 2, lines 19-40.

Regarding claim 16, Grill discloses the semiconductor device further including, over each of the first and second interconnects, a selective metal deposition layer 290

comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer. Se figs. 3.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 4-6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,413,852 to Grill et al., in view of the following remarks.

Regarding claim 4, Grill discloses the semiconductor device further including, beneath the at least one of the first and second interconnects, an etch stop layer 110, positioned over an underlying via insulator level.

Grill is silent about a correspondence of the thickness of the etch stop layer and the distance the air gap extending below the lower surface of the interconnects.

However, Grill does teach that the air gap 270/270' extends below the lower surface of the at least one of the first and second interconnects 185 by a distance corresponding to a thickness of the diffusion barrier 170. See figs. 1N-P, figs. 3A-B, figs. 4C-D, and figs. 5D.

Therefore, it would have been an obvious to one of ordinary skills in the art that the diffusion barrier 170 and the etch stop layer 110 can be formed with respective thicknesses corresponding to each other, hence, the distance the air gap extending below the lower surface of the interconnects would be corresponding to the thickness of the etch stop layer, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claim 5, Grill discloses the semiconductor device wherein the etch stop layer comprises silicon carbide. See col. 4, line 63 to col. 5, line 24; col. 6, lines 22-44.

Regarding claim 6, Grill discloses the semiconductor device wherein the underlying via insulator level comprises silicon dioxide or fluorinated silicon dioxide. See col. 4, line 63 to col. 5, line 24; col. 6, lines 22-44.

Conclusion

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
October 3, 2005